REMARKS

Applicants respectfully request reconsideration of the present application as currently amended.

Claims 1-22 are pending in the present application.

Claims 1-8, and 16-22 are rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter.

Claims 1-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,878,258 of Pizi et al. ("Pizi") in view of U.S. Patent No. 5,694,581 of Cheng ("Cheng").

Claims 1, 9, and 16-22 have been amended. Support for the amendment in those amended claims can be found in the application as originally filed. For example, support for amended claim 1 can be found in Figures 2-3 and 5, and in the specification at paragraphs 0019, 0023, and 0037-0050. Applicants submit that no new matter has been added.

The Office Action mailed 06/22/2010 has rejected claims 1-8 and 16-22 under 35 U.S.C. 101. The Office Action states in part that

> As per claims 1, it recites a "system"; however, it appears that the system would reasonably be interpreted by one of ordinary skill in the art as software, per se, failing to be tangibly embodied or include any recited hardware as part of the system. Software alone is directed to a non-statutory subject matter. Applicant is advised to amend the claims to include a hardware (i.e., processor and memory) to overcome the 101 rejection.
>
> ...
>
> Claim 16 is a computer program product claim that appearing to be comprised of software alone without claiming associated computer hardware required for storing and executing the program product. Applicant is suggested to amend the preamble of the claim to include "computer program product stored in a memory and executed by a processor to overcome the outstanding 101 rejection.

(06/22/2010 Office Action, pp. 2-3).

As stated above, claims 1, 9, and 16-22 have been amended. In particular, claim 1 has been amended to, as suggested by the Examiner, recite a computer system with a processor and a

memory, in addition to the BIOS system. Moreover, claim 16 has been amended to recite a "computer readable storage storing a computer program that can be executed by a processor and that include sequences of instructions, the sequences of instructions including instructions which, when executed by the processor, cause the processor to perform a method of synchronizing concurrent resource accesses by a plurality of routines in a basic input and output system (BIOS) of a computer system". It is submitted that above mentioned claim amendments overcome the Examiner's rejection under 35 U.S.C. §101.

The Office Action mailed 06/22/2010 has rejected claims 1-22 under 35 U.S.C. §103(a) as being unpatentable over Pizi in view of Cheng. In particular, The Office Action states in part that

> As per claims 1-2, 5-6, 9, 16, Pizi teaches a method of synchronizing resource accesses in a computer system, comprising:
>
> associating an access indicator with each of a plurality of resources (Column 10, lines 50-51);
>
> determining when current value an access indicator of a resource has when a routine wants to access that resource, wherein the value of the access indicator indicates how many routines are allowed to access the resource concurrently; and changing the value of the access indicator by a predetermined amount and granting access to the resource to the requesting routine if the value is not at a predetermined level (Column 2, lines 27-30; Column 10, lines 47-60: it is obvious that the indicator changes count value when a routine accesses the resource).
>
> Pizi does not specifically teach that the resource access happens in a BIOS and that the access is current.
>
> However, Pizi does teach that the applications running in his system are running concurrently and since such application often has the need to access the resource currently, in that event, one would result in a situation where Pizi's applications accessing the resources concurrently. Furthermore, Cheng teaches a situation where concurrent resource accesses are performed in a BIOS environment for the purpose of easier information retrieval (abstract).

(06/22/2010 Office Action, pp. 3-4).

Applicants respectfully disagree.

It is submitted that the combination of Pizi and Cheng does not render claims 1-22, as amended, unpatentable under 35 U.S.C. §103(a).

Pizi includes a disclosure of having a computer interface program provide for subordination of select operating system and application commands. The system permits a seamless integration of distinct applications with a common context controller that permits inter-application communication regarding the operating environment. System resources are managed to insure critical operations retain priority, while permitting access to resources as they are freed by the system (see Pizi Abstract). From column 10, line 24 to column 12, line 13 of Pizi further discloses a resource allocation process that employs a reference counter for each resource.

The Office Action mailed 06/22/2010 admits that Pizi does not teach that the resource access happens in a BIOS and that the access is concurrent. In addition, it is noted that Pizi does not simply teach or suggest any synchronization of concurrent running of routines. Nowhere in Pizi teaches or suggests synchronization of concurrent running of routines (see Pizi the entire document). The sections of Pizi relied on by the Examiner in his Office Action in rejecting claims 1-22 (i.e., columns 10-11) disclose only a reference counter for resource allocation purposes (i.e., how many applications can share a resource so the resource is not over subscribed).

Cheng includes a disclosure of disk array access management system connected between a host computer and at least two independent concurrently operational disk arrays. The management system includes a concurrent disk array interface device for interfacing with concurrent disk arrays for performing concurrent disk accesses from the host computer to the disks (see Cheng Abstract).

Although Cheng mentions concurrent data transfer operations via two disk array channels, Cheng fails to disclose, teach, or suggest that they are synchronized concurrent operations. Nowhere in Cheng is the feature of synchronized concurrent operation with concurrent resource accesses mentioned, described, taught, or suggested (see Cheng the entire

document). Instead, the disk arrays in Cheng are independent concurrently operational disk arrays for independent concurrent operations (Emphasis Added)(see Cheng Abstract and column 4, lines 1-3 and 16-23 and column 5, lines 53-63). This means that they are not (and do not need to be) synchronized.

It is submitted that the combination of Pizi and Cheng does not render claim 1, as amended, unpatentable under 35 U.S.C. §103(a) as neither Pizi nor Cheng discloses, teaches, or suggests a synchronization module to synchronize concurrent running of the routines that include concurrent resource accesses to different ones of the resources, wherein the synchronization module allows for the concurrent running of the routines with the concurrent resource accesses to different ones of the resources by blocking competing concurrent resource accesses while permitting (1) non-competing concurrent resource accesses and (2) non-resource access operations (Emphasis Added).

Specifically, Pizi simply does not disclose, teach, or suggest a synchronization module to synchronize concurrent running of routines with concurrent resource accesses. The Office Action mailed 06/22/2010 admits that Pizi does not teach that the resource access happens in a BIOS and that the access is concurrent. In addition, nowhere in Pizi teaches or suggests synchronization of concurrent running of routines with concurrent resource accesses. The sections of Pizi relied on by the Examiner (i.e., columns 10-11) disclose only a reference counter for resource allocation purposes (i.e., how many applications can share a resource so the resource is not over subscribed).

Likewise, although Cheng mentions concurrent data transfer operations via two disk array channels, the disk arrays in Cheng are independent concurrently operational disk arrays (Emphasis Added)(see Cheng Abstract and column 4, lines 1-3 and 16-23 and column 5, lines 53-63). This means that it is not necessary, in Cheng, to have the concurrent operations synchronized. Thus, Cheng teaches or suggests away having such a synchronization module as the concurrent operational disk arrays in Cheng are independent to each other, making it

unnecessary to have the concurrent operations synchronized.

In contrast, amended claim 1 states in part that

> a synchronization module to synchronize concurrent running of the routines that include concurrent resource accesses to different ones of the resources, wherein the synchronization module allows for the concurrent running of the routines with the concurrent resource accesses to different ones of the resources by blocking competing concurrent resource accesses while permitting (1) non-competing concurrent resource accesses and (2) non-resource access operations.

(Amended claim 1) (Emphasis added).

Given that claims 2-8 depend from amended claim 1, it is likewise submitted that these claims are also patentable under 35 U.S.C. §103(a) over Pizi and Cheng.

It is submitted that the combination of Pizi and Cheng does not render amended claims 9 and 16 unpatentable under 35 U.S.C. §103(a) as neither Pizi nor Cheng discloses, teaches, or suggests synchronizing concurrent running of the routines such that routines that have been granted accesses to their corresponding resources and routines that do not require resource access run concurrently (Emphasis Added).

To the contrary, Pizi does not disclose, teach, or suggest synchronizing concurrent running of routines with concurrent resource accesses. The Office Action mailed 06/22/2010 admits that Pizi does not teach that the resource access happens in a BIOS and that the access is concurrent. In addition, nowhere in Pizi teaches or suggests synchronization of concurrent running of routines with concurrent resource accesses. The sections of Pizi relied on by the Examiner (i.e., columns 10-11) disclose only a resource allocation operation with a reference counter to control how many applications can share a resource so the resource is not over subscribed.

Likewise, although Cheng mentions concurrent data transfer operations via two disk array channels, the disk arrays in Cheng are independent concurrently operational disk arrays (Emphasis Added)(see Cheng Abstract and column 4, lines 1-3 and 16-23 and column 5, lines 53-

63). This means that it is not necessary, in Cheng, to have the concurrent operations synchronized. Thus, Cheng teaches or suggests away such a synchronization operation as claimed in amended claim 9 as the concurrent operational disk arrays in Cheng are independent to each other, making it unnecessary to have the concurrent operations synchronized.

In contrast, amended claim 9 states in part that

> A method of synchronizing concurrent resource accesses by a plurality of routines in a basic input and output system (BIOS) of a computer system, comprising:
> ...
> synchronizing concurrent running of the routines such that routines that have been granted accesses to their corresponding resources and routines that do not require resource access run concurrently.

(Amended claim 9)(Emphasis Added). Amended claim 16 includes similar limitations.

Given that claims 10-15 and 17-22, as amended, depend from amended claims 9 and 16, respectively, it is likewise submitted that these claims are also patentable under 35 U.S.C. §103(a) over Pizi and Cheng.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-22, as amended, should be found to be in condition for allowance.

The Examiner is invited to telephone Applicants' attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 21st day of September, 2010.

Christine Hartness